

WHAT IS CLAIMED IS:

1 1. A method of executing an instruction comprising:
2 receiving residual data of a first image and decoded pixels of a second image;
3 zero-extending a plurality of unsigned data operands of the decoded pixels
4 producing a plurality of unpacked data operands;
5 adding a plurality of signed data operands of the residual data to the plurality of
6 unpacked data operands producing a plurality of signed results;
7 saturating the plurality of signed results producing a plurality of unsigned results.

8 2. The method as recited in Claim 1, wherein the residual data comprises data
9 results from an inverse discrete cosine transform (DCT) operation and the second image
10 comprises a previously decoded video frame.

11 3. The method as recited in Claim 1, wherein the second image is an earlier
12 decoded block from a same video frame as the first image.

13 4. The method as recited in Claim 1, wherein the zero-extending, the adding and
14 the saturating are part of a video estimation function.

15 5. The method as recited in Claim 1, wherein the zero-extending, the adding and
16 the saturating are part of a video compensation function.

17 6. The method as recited in Claim 1, wherein the instruction is a Single-
18 Instruction/Multiple-Data (SIMD) instruction.

19 7. The method as recited in Claim 1, wherein the method comprises executing a
20 Single-Instruction/Multiple-Data (SIMD) instruction.

21 8. The method as recited in Claim 1, wherein the method is performed utilizing
22 Single-Instruction/Multiple-Data (SIMD) circuitry.

23 9. A method comprising:

24 decoding an instruction identifying a mixed-mode addition operation;

25 executing the instruction on a first source and a second source, wherein the first

26 source comprises a plurality of signed residual data of a first image and

27 the second source comprises a plurality of unsigned decoded pixels of a

28 second image; and

29 storing an output of the executing the instruction, wherein the output comprises a

30 plurality of unsigned result pixels;

31 wherein the executing the instruction comprises:

32 zero-extending at least one of the plurality of unsigned decoded pixels;

33 adding the at least one of the plurality of unsigned decoded pixels and the

34 plurality of signed residual data producing a plurality of signed

35 sums; and

36 saturating the plurality of signed sums producing the plurality of unsigned

37 result pixels.

38 10. The method as recited in Claim 9, further comprising:

39 executing the instruction on a third source and at least one other of the plurality of

40 unsigned decoded pixels of the second source, wherein the third source

41 comprises another plurality of signed residual data, wherein the executing

42 produces another plurality of unsigned result pixels;

43 storing the another plurality of unsigned result pixels; and
44 performing an OR operation on the plurality of unsigned result pixels and the
45 another plurality of unsigned result pixels, and storing a plurality of OR
46 results into a single destination register.

47 11. The method as recited in Claim 9, wherein the plurality of signed residual data
48 comprises data results from an inverse discrete cosine transform (DCT) operation and the
49 second image comprises a previously decoded video frame.

50 12. The method as recited in Claim 9, wherein the zero-extending, the adding and
51 the saturating are part of a video compensation function.

52 13. The method as recited in Claim 9, wherein the instruction is a Single-
53 Instruction/Multiple-Data (SIMD) instruction.

54 14. An apparatus comprising:
55 a first plurality of multiplexers, each multiplexer of the first plurality of
56 multiplexers operative to select one of a plurality of unsigned decoded
57 pixels and zero-extend the unsigned decoded pixels, the first plurality of
58 multiplexers operative to produce a plurality of unpacked operands;
59 a plurality of adders, each adder of the plurality of adders operative to add a
60 signed residual data operand to one of the plurality of unpacked operands,
61 the plurality of adders operative to produce a plurality of sums,
62 a plurality of saturation units operative to produce a plurality of unsigned result
63 pixels from the plurality of sums.

64 15. The apparatus as recited in Claim 14, further comprising:

65 a second plurality of multiplexers operative to select between the plurality of
66 unsigned result pixels and zeroes.

67 16. The apparatus as recited in Claim 14, wherein the plurality of adders
68 comprises four 16-bit adders.

69 17. The apparatus as recited in Claim 14, wherein selection controls for the first
70 plurality of multiplexers is according to a qualifier specified in a Single-
71 Instruction/Multiple-Data (SIMD) instruction.

72 18. The apparatus as recited in Claim 14, wherein configuration of the first
73 plurality of multiplexers, the plurality of adders, and the plurality of saturation units is
74 selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD)
75 instruction.

76 19. The apparatus as recited in Claim 14, wherein configuration of the first
77 plurality of multiplexers, the plurality of adders, and the plurality of saturation units is
78 selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD)
79 instruction.

80 20. The apparatus as recited in Claim 14, wherein the first plurality of
81 multiplexers, the plurality of adders, and the plurality of saturation units form a Single-
82 Instruction/Multiple-Data (SIMD) instruction execution circuit.

83 21. The apparatus as recited in Claim 14, wherein the signed residual data
84 operand comprises data results from an inverse discrete cosine transform (DCT)

operation and the unsigned decoded pixels comprise a portion of a previously decoded video frame.

22. The apparatus as recited in Claim 21, wherein the apparatus is utilized by a video compensation function.

23. An apparatus comprising:

a coprocessor interface unit to identify an instruction for a mixed-mode operation,

a first source having a plurality of signed residual data operands and a

second source having a plurality of unsigned decoded pixels;

an execution unit to perform the mixed-mode operation on the plurality of signed

residual data operands and the plurality of unsigned decoded pixels; and

a register to store a result having a plurality of unsigned result pixels;

wherein the execution unit comprises:

a first plurality of multiplexers, each multiplexer of the first

plurality of multiplexers operative to select one of the plurality of

unsigned decoded pixels and zero-extend the unsigned decoded pixels, the

first plurality of multiplexers operative to produce a plurality of unpacked

operands;

a plurality of adders, each adder of the plurality of adders operative

to add one of the plurality of signed residual data operands and one of the

plurality of unpacked operands, the plurality of adders operative to

produce a plurality of signed sums, and

a plurality of saturation units operative to produce a plurality of

unsigned result pixels from the plurality of signed sums.

24. The apparatus as recited in Claim 23, the execution unit further comprising:

109 a second plurality of multiplexers operative to select between the plurality of
110 unsigned result pixels and zeroes.

111 25. The apparatus as recited in Claim 23, wherein the plurality of adders
112 comprises four 16-bit adders.

113 26. The apparatus as recited in Claim 23, wherein selection controls for the first
114 plurality of multiplexers is according to a qualifier specified in a Single-
115 Instruction/Multiple-Data (SIMD) instruction.

116 27. The apparatus as recited in Claim 23, wherein configuration of the first
117 plurality of multiplexers, the plurality of adders, and the plurality of saturation units is
118 selected according to microcode identified by a Single-Instruction/Multiple-Data (SIMD)
119 instruction.

120 28. The apparatus as recited in Claim 23, wherein configuration of the first
121 plurality of multiplexers, the plurality of adders, and the plurality of saturation units is
122 selected according to decode logic and a Single-Instruction/Multiple-Data (SIMD)
123 instruction.

124 29. The apparatus as recited in Claim 23, wherein the signed residual data
125 operands comprise data results from an inverse discrete cosine transform (DCT)
126 operation and the unsigned decoded pixels comprise a portion of a previously decoded
127 video frame.

128 30. A data processing system comprising:

an addressable memory to store an instruction for a mixed-mode operation;
a processing core coupled to the addressable memory, the processor core
comprising:
an execution core to access the instruction;
a first source register to store a plurality of signed residual data operands;
a second source register to store a plurality of unsigned decoded pixels;
and
a destination register to store a plurality of unsigned result pixels;
a wireless interface to receive an encoded bit stream; and
an I/O system and decoder to provide the plurality of signed residual data
operands to the first source register from the encoded bit stream;
wherein the execution core comprises:
a first plurality of multiplexers, each multiplexer of the first
plurality of multiplexers operative to select one of the plurality of
unsigned decoded pixels and zero-extend the unsigned decoded pixels, the
first plurality of multiplexers operative to produce a plurality of unpacked
operands;
a plurality of adders, each adder of the plurality of adders operative
to add a signed residual data operand to one of the unpacked operands, the
plurality of adders operative to produce a plurality of sums, and
a plurality of saturation units operative to produce a plurality of
unsigned result pixels.

31. The data processing system as recited in Claim 30, wherein the plurality of
adders comprises four 16-bit adders.

153 32. The data processing system as recited in Claim 30, wherein the I/O system
154 and decoder comprise an inverse discrete cosine transform function.

155 33. The data processing system as recited in Claim 30, wherein selection controls
156 for the first plurality of multiplexers is according to a qualifier specified in a Single-
157 Instruction/Multiple-Data (SIMD) instruction.

158 34. The data processing system as recited in Claim 30, wherein configuration of
159 the first plurality of multiplexers, the plurality of adders, and the plurality of saturation
160 units is selected according to microcode identified by a Single-Instruction/Multiple-Data
161 (SIMD) instruction.

162 35. The data processing system as recited in Claim 30, wherein configuration of
163 the first multiplexer, the adders, and the saturation units is selected according to decode
164 logic and a Single-Instruction/Multiple-Data (SIMD) instruction.

165 36. The data processing system as recited in Claim 30, wherein the signed
166 residual data operands comprise data results from an inverse discrete cosine transform
167 (DCT) operation and the unsigned decoded pixels comprise a portion of a previously
168 decoded video frame.